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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TSAI, HENRY	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,971	GAITHER ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on __________ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Neufeld (U.S. Patent No. 6,567,901) (hereafter referred to as Neufeld'901).

Referring to claim 1, Neufeld'901 discloses, as claimed, a method for processing a memory access request within processing architecture, comprising the steps of: determining whether the memory access request is speculative or not based upon a first identifier (<u>a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could</u>

be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction"); assessing one or both of interconnect (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability) and target resource conditions (see Fig. 4, since memory requests, such as 421, 422, 417, and 419 are processed, see also Col. 5, lines 47-50 for the memory requests 417 and 419 with the corresponding status of value speculative. Note for processing a speculative memory request such as 421 (see Col. 5, lines 51-53), the memory request processing logic 442 certainly assess (or check) the target resource condition in order to complete the speculative memory request 421, see Fig. 4 and Col. 5, lines 56-60) in the event that the memory access request is speculative; and either processing the request, or not (see Col. 5, lines 65-67, and col. 6, lines 1-2, when the memory request such as memory request 421 is cancelled), as a function of the conditions (note processing the speculative memory request 421 (see Col. 5, lines 51-53) is based on: a function of interconnect (as set forth, see Col. 6, lines 29-30, since the transactions are delivered

sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability); and /or a function of the target conditions since the memory request processing logic 442 certainly will base on the target resource condition in order to complete the memory request 421 or not, see Col. 5, lines 56-60).

Referring to claim 14, Neufeld'901 discloses, as claimed, in CPU architecture (processor 30, see Fig. 4) that initiates both speculative and non-speculative memory access requests (see Fig. 3, and Fig. 4, memory requests, such as 421, 422, 417, and 419 are processed), an improvement comprising decode logic for determining whether the memory access requests are speculative (decoding a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction"), and assessment logic for determining one or both of interconnect (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability) and

target resource conditions (see Fig. 4, since memory requests, such as 421, 422, 417, and 419 are processed, see also Col. 5, lines 47-50 for the memory requests 417 and 419 with the corresponding status of value speculative. Note for processing a speculative memory request such as 421 (see Col. 5, lines 51-53), the memory request processing logic 442 certainly assess (or check) the target resource condition in order to complete the speculative memory request 421, see Fig. 4 and Col. 5, lines 56-60), the CPU architecture (processor 30, see Fig. 4) processing speculative requests, or not (see Col. 5, lines 65-67, and col. 6, lines 1-2, when the memory request such as 421 is cancelled), as a function of the conditions (note processing the speculative memory request 421 (see Col. 5, lines 51-53) is based on: a function of interconnect (as set forth, see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability); and/or a function of the target conditions since the memory request processing logic 442 certainly will base on the target resource condition in order to complete the memory request 421 or not, see Col. 5, lines 56-60).

Referring to claim 16, Neufeld'901 discloses, as claimed, a system for processing speculative memory access requests within

a processing architecture, comprising: one or more requests having a bit field (a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction") defining the requests as speculative or non-speculative; decode logic (inherently existing inside the processor 30, se Fig. 1) for decoding the bit field to determine whether one or more memory access requests are speculative; and processing logic (inherently existing inside the processor 30, se Fig. 1) for processing speculative memory access requests, or not, based on at least one of interconnect (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability) and target resource conditions (note processing the speculative memory request 421 (see Col. 5, lines 51-53) is based on: a function of interconnect (as set forth, see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its

availability); and/or a function of the target conditions since the memory request processing logic 442 certainly will base on the target resource condition in order to complete the memory request 421 or not, see Col. 5, lines 56-60).

As to claim 2, Neufeld'901 also discloses the step of determining whether the request is speculative comprises decoding first identifier as a first bit field (as set forth, a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction") within the memory access request.

As to claim 3, Neufeld'901 also discloses encoding the **first bit field (as set forth, a bit encoded in the instruction, see Col. 4, lines 9-15,** regarding "the instruction set of the **processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit** encoded in the instruction") within the **memory access request to define a speculative ID of the memory access request.**

As to claim 4, Neufeld'901 also discloses the memory access request comprising one of an instruction, message and operational request (the memory requests, such as 421, and 422 shown in Fig. 4).

As to claim 5, Neufeld'901 also discloses the step of determining a priority (see Col. 6, lines 28-30, regarding "a multiplexing of the priority with the transactions"; and Col. 6, lines 40-43, regarding "by prioritizing memory requests over a bus based on status information") of the memory access request based upon a second identifier (see Col. 4, lines 16-24, regarding "an additional status"), in the event that the memory access request is speculative, and wherein the step of processing the request comprises processing the memory access request (the memory requests, such as 421, and 422 shown in Fig. 4), or not, based upon the conditions and the priority (note for processing a memory request as a function of the conditions and the priority is an inherent step, see also Col. 5, lines 41-67, and col. 6, lines 1-2, for processing the memory request 421 as a function of the conditions, the memory request 421 may be cancelled based on the conditions).

As to claim 6, Neufeld'901 also discloses the step of determining a priority comprises decoding the second identifier (see Col. 4, lines 16-24, regarding "an additional status") as a

second bit field within the memory access request (the memory requests, such as 421, and 422 shown in Fig. 4).

As to claim 7, Neufeld'901 also discloses comprising encoding the second bit field (see Col. 4, lines 16-24, regarding "an additional status", the second bit field is inherently in the additional status) within the memory access request to define a priority of the memory access request.

As to claims 8, and 18, Neufeld'901 also discloses the memory access request comprises one of a memory read request and a memory load request (the memory requests, such as 421, and 422 shown in Fig. 4).

As to claims 9, and 17, Neufeld'901 also discloses the step of determining comprises utilizing one of a CPU (the processor 30, see Fig. 4), chipset and memory controller (the memory controller 14, see Fig. 2) to determine whether the memory access request (the memory requests, such as 421, and 422 shown in Fig. 4) is speculative.

As to claim 10, Neufeld'901 also discloses at least one of the CPU (the processor 30, see Fig. 4), chipset and memory controller (the memory controller 14, see Fig. 2) independently controls the step of processing the memory access request (the memory requests, such as 421, and 422 shown in Fig. 4) based on the conditions.

As to claim 11, Neufeld'901 also discloses the step of assessing target resource conditions comprises assessing one or more of memory utilization, memory congestion (since the request to be processed are the memory requests, such as 421, and 422 shown in Fig. 4), buffer space utilization (see memory request queue 401 in Fig. 4), and bus congestion (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus).

As to claim 12, Neufeld'901 also discloses the step of assessing interconnect conditions comprises assessing one or more of bus utilization, bus congestion (see col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus), crossbar utilization, cross bar congestion, and point to point link utilization.

As to claim 13, Neufeld'901 also discloses comprising the step of notifying one or more logic devices (such as memory request processing logic 442, see Fig. 4) when the memory access request is not processed (such as the memory request 421 is cancelled, see col. 5, lines 65-67 and Col. 6, lines 1-2).

As to claim 15, Neufeld'901 also discloses a prefetch unit (inherently existing inside the processor 30, se Fig. 1) for prefetching speculative requests (such as the speculative read in the instruction 304, see Fig. 3), wherein the decode logic

detects (by detecting a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction") whether prefetched requests are speculative.

As to claim 19, Neufeld'901 also discloses a bus controller (inherently existing inside the processor 30, se Fig. 1) for assessing one or more of bus congestion and bus utilization conditions.

Response to Amendment

3. Applicant's arguments filed 9/29/04 have been fully considered but they are not deemed to be persuasive.

Regarding the limitations in claim 1, Applicants argue that "In step b), claim 1 specifically requires that one or both of the interconnect and target resource conditions is assessed to determine if a speculative memory access request is processed. Neufeld'901 does not teach or suggest this feature, at least, and therefore cannot anticipate claim 1"; and

"However, this assessment is by protocol, and does not determine **if `traffic on bus 30 is too congested' or that `target memory ... is saturated' - as in the '971 Application. Such a protocol does not therefore include decision logic that may postpone or abort processing of a speculative memory request".** Examiner disagrees with Applicants. As set forth in the art rejections, Neufeld'901 discloses: assessing one or both of interconnect (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability) and target resource conditions (see Fig. 4, since memory requests, such as 421, 422, 417, and 419 are processed, see also Col. 5, lines 47-50 for the memory requests 417 and 419 with the corresponding status of value speculative. Note for processing a speculative memory request such as 421 (see Col. 5, lines 51-53), the memory request processing logic 442 certainly assess (or check) the target resource condition in order to complete the speculative memory request 421, see Fig. 4 and Col. 5, lines 56-60) in the event that the memory access request is speculative.

Regarding the limitations in claims 2-9, Applicants argue that these claims have additional reasons for patentability. Examiner disagrees with Applicants. As set forth in the art

rejections, Neufeld'901 discloses the limitations as described in claims 2-9.

Regarding the limitations in claim 10, Applicants argue that "In addition, note that amended claim 10 recites that at **least one of the CPU, chipset and memory controller independently controls the step of processing the memory access request based on the conditions. Neufeld'901 does not teach of** processing the memory access request based on such conditions"; and "**Neufeld'901 also does not consider bus traffic and target resource congestion. The use of a communication protocol on a bus cannot reasonably anticipate the assessment of bus traffic conditions or target resource congestion as described in the '971 Application**". Examiner disagrees with Applicants. As set forth in the art rejections, Neufeld'901 discloses at least one of the CPU (<u>the processor 30, see Fig. 4</u>), chipset and memory controller (<u>the memory controller 14, see Fig. 2</u>) independently controls the step of processing the memory access request (<u>the memory requests, such as 421, and 422 shown in Fig. 4</u>) based on the conditions.

Regarding the limitations in claims 11 and 12, Applicants argue that "Neufeld'901 does not teach of monitoring memory **utilization, memory congestion, buffer space utilization or bus congestion. Accordingly, Neufeld'901 does not, again, anticipate**

claims 11, 12". Examiner disagrees with Applicants. As set forth in the art rejections, Neufeld'901 discloses: the step of assessing target resource conditions comprises assessing one or more of memory utilization, memory congestion (since the request to be processed are the memory requests, such as 421, and 422 shown in Fig. 4), buffer space utilization (see memory request queue 401 in Fig. 4), and bus congestion (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus); and the step of assessing interconnect conditions comprises assessing one or more of bus utilization, bus congestion (see col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus), crossbar utilization, cross bar congestion, and point to point link utilization.

Regarding the limitations in claim 13, Applicants argue that "according to Neufeld'901, a first speculative request is issued to the memory controller, and, later, the processor may send a second request to inform the memory controller not to process the first speculative request". Examiner realizes the Neufeld'901's feature as described. However, as described in the claim, Neufeld'901 also discloses comprising the step of notifying one or more logic devices (such as memory request processing logic 442, see Fig. 4) when the memory access request

is not processed (such as the memory request 421 is cancelled, see col. 5, lines 65-67 and Col. 6, lines 1-2).

Regarding the limitations in claim 14, Applicants argue that "Neufeld'901 does not teach utilizing conditions of the interconnect or target resource. Neufeld'901 also teaches away from the present inventions (in each independent claim) in that it is the processor that generates instructions to change the status of, or to delete, speculative requests. See Neufeld'901, col. 5, lines 56-67, col. 6, lines 1-2". Examiner disagrees with Applicants. As set forth in the art rejections, Neufeld'901 discloses: an improvement comprising decode logic for determining whether the memory access requests are speculative (decoding a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction"), and assessment logic for determining one or both of interconnect (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability) and target resource conditions (see Fig. 4, since

memory requests, such as 421, 422, 417, and 419 are processed, see also Col. 5, lines 47-50 for the memory requests 417 and 419 with the corresponding status of value speculative. Note for processing a speculative memory request such as 421 (see Col. 5, lines 51-53), the memory request processing logic 442 certainly assess (or check) the target resource condition in order to complete the speculative memory request 421, see Fig. 4 and Col. 5, lines 56-60).

Regarding the limitations in claim 16, Applicants argue that "Neufeld'901 does not teach or suggest processing logic for processing speculative requests, or not, based on at least one of interconnect and target resource conditions"; and "We contend that assessing the target resource or the interconnect condition to determine if the target resource is saturated, or if the interconnect is congested [e.g., see the '971 Application, paragraph 31], is not inherent to processing speculative requests as disclosed by Neufeld'901". Examiner disagrees with Applicants. As set forth in the art rejections, Neufeld'901 discloses: as claimed, a system for processing speculative memory access requests within a processing architecture, comprising: one or more requests having a bit field (a bit encoded in the instruction, see Col. 4, lines 9-15, regarding "the instruction set of the processor 30 could be such that a

compiler could predetermine the speculative or non-speculative native of the transaction 305 and pass that information to the processor 30, such as with a bit encoded in the instruction") defining the requests as speculative or non-speculative; decode logic (inherently existing inside the processor 30, se Fig. 1) for decoding the bit field to determine whether one or more memory access requests are speculative; and processing logic (inherently existing inside the processor 30, se Fig. 1) for processing speculative memory access requests, or not, based on at least one of interconnect (see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability) and target resource conditions (note processing the speculative memory request 421 (see Col. 5, lines 51-53) is based on: a function of interconnect (as set forth, see Col. 6, lines 29-30, since the transactions are delivered sequentially over a single bus. Neufeld'901' system assesses the single bus interconnect such as traffic condition in order to determine its availability); and/or a function of the target conditions since the memory request processing logic 442 certainly will base on the target resource condition in order to complete the memory request 421 or not, see Col. 5, lines 56-60).

Regarding the limitations in claims 17 and 19, Applicants also argue that "Neufeld'941 simply does not teach or disclose such decode and processing logic"; and "Neufeld'901 does not teach assessing bus congestion and bus utilization conditions for purposes of determining if speculative requests are processed or not". Examiner disagrees with Applicants. The teaching from Neufeld'901 for the limitations are clearly explained in the art rejections as set forth above.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated

from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, (571) 272-2100.**

6. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly **into the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account.

Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

Henry Tsai

HENRY W. H. TSAI
PRIMARY EXAMINER

November 14, 2004